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am a translator of the documents attached, and state that the following is a true translation to the best of my knowledge and belief of Japanese Patent Application Number 2002-302689.

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[Title of the Invention] MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE

[Scope of Patent Claims]

[Claim 1] A manufacturing method of a semiconductor device in which wiring made of metal is formed of a single layer structure or a multilayer structure, characterized in that:

an interlayer insulating film for electrically isolating the wirings from each other located above and below or side by side is formed of an SiOC film; and a SiC film with a thickness of 5 nm or more is formed so as to come into cntact with said SiOC.

[Claim 2] A manufacturing method of a semiconductor device in which wiring made of metal is comprised of a single layer structure or a multilayer structure, characterized in that:

an interlayer insulating film for electrically isolating the wirings from each other located above and below or side by side is formed of an SiOC film which contains nitrogen; and a relatively thin SiCN film with a nitrogen content of 1% or less is formed so as to come into contact with said SiOC film.

[Claim 3]

A manufacturing method of a semiconductor device in which wiring made of metal is formed of a single layer structure or a multilayer structure, characterized in that:

an interlayer insulating film for electrically isolating the wirings from each other located above and below or side by side is formed of an SiOC film; and an insulating film having the difference in Young's modulus from said SiOC film of 50 GPa or less or the difference in stress from said SiOC film of 50

MPa or less is formed so as to come into contact with said SiOC film.

[Claim 4]

A manufacturing method of a semiconductor device in which wiring made of metal is formed of a single layer structure or a multilayer structure, characterized in that:

an interlayer insulating film for electrically isolating the wirings from each other located above and below or side by side is formed of an SiOC film; an relatively thin SiCN film is formed on or below said SiOC film; and an SiC film with a thickness of 5 nm or larger is interposed between said SiOC film and said SiCN film.

[Claim 5]

A manufacturing method of a semiconductor device in which wiring made of metal is comprised of a single layer structure or a multilayer structure, characterized in that:

an interlayer insulating film for electrically isolating the wirings from each other located above and below or side by side is formed of an SiOC film which contains nitrogen; and a relatively thin SiCN film is formed so as to come into contact with said SiOC film.

[Detailed Explanation of the Invention]

[Technical Field]

[0001]

[Technical Field of the Invention]

The present invention relates to a technique for manufacturing a semiconductor device. More particularly, the present invention relates to a technique effectively applied to a wiring structure formed by the so-called damascene process

and to a semiconductor device with such a wiring structure.

[0002]

[Prior Art]

In order to suppress the wiring delay caused by the scaling down of the semiconductor device, the attempts to reduce the wiring resistance and the wiring capacitance have been made. With respect to the wiring resistance, the measures by means of design technique and the adoption of the wiring made of copper to be a main conductor layer have been examined. For the formation of the copper wiring, the so-called damascene process is employed, in which metal for the wiring such as copper to be the main conductor layer is deposited on a substrate and on the surface of the trenches formed in an insulating film and then the superfluous metal outside the trenches is removed by the CMP (Chemical Mechanical Polishing) method, thus forming the wiring patterns in the trenches.

[0003]

Meanwhile, with respect to the wiring capacitance, the adoption of the low dielectric constant material with the relatively low relative dielectric constant of about 2 to 3 has been examined. Above all, the film made of silicon-oxycarbite (referred to as SiOC, hereinafter) which is excellent in mechanical strength is considered as a promising low dielectric constant material.

[0004]

Note that Japanese Patent Laid-Open No. 2001-326279 discloses the technique, in which the insulating film that comes into contact with the copper wiring of the multilayered insulating film constituting the interlayer insulating film is

formed by plasmanizing the film forming gas containing the alkyl compound having the siloxane bond and any one oxygen-containing gas of N_2O, H_2O, and CO_2, whose flow rate is equal to or less than the flow rate of the alkyl compound, and then reacting them mutually.

[0005]

Also, Japanese Patent Laid-Open No. 2001-110789 discloses the method of depositing and etching the intermetallic dielectric layer comprised of the first dielectric layer containing silicon, oxygen, and about 5% of carbon by atomic weight and the second dielectric layer containing silicon, oxygen, and about two-thirds or less of the carbon contained in the first dielectric layer.

[0006]

[Problems to be solved by the Invention]

The inventors of the present invention have examined the manufacturing method of the damascene wiring. The technique examined by the inventors of the prevent invention will be shown below, and the summary thereof will be provided as follows.

[0007]

First, a stopper insulating film and an insulating film for forming the wiring (referred to as film between wiring layers, hereinafter) are sequentially deposited. The film between wiring layers is comprised of an SiOC film formed by the plasma CVD (Chemical Vapor Deposition) method, and the stopper insulating film is comprised of a silicon oxide (referred to as SiO, hereinafter) film, a silicon nitride (referred to as SiN, hereinafter) film, or a silicon

carbonitride (referred to as SiCN, hereinafter) film formed by, for example, the plasma CVD method. The stopper insulating film functions as an etching stopper layer in the etching of the film between wiring layers.

[0008]

Next, the wiring trenches are formed in the predetermined region of the film between wiring layers and the stopper insulating film by the etching with using the patterned photoresist film as a mask. Subsequently, a barrier film, for example, a titanium nitride film is formed on the entire surface of the substrate including the surface of the wiring trenches, and then, a copper film for filling the wiring trenches is formed. The copper film functions as a main conductor layer and can be formed by, for example, the plating method. Thereafter, the copper film and the barrier layer in the region outside the wiring trenches are removed by the CMP method, thus forming the copper wiring in the wiring trenches.

[0009]

Next, a cap insulating film functioning as a barrier layer is formed on the copper wiring in order to prevent the diffusion of the copper from the copper wiring. The cap insulating film is comprised of, for example, an SiO film, an SiN film, or an SiCN film formed by the plasma CVD method. In addition to the function as a barrier layer, the cap insulating film has a function as an etching stopper layer when forming connection holes in the insulating film on the copper wiring.

[0010]

However, as a result of the examination of the scaling down of the damascene wiring with the process dimensions of 0.1

μm or smaller with the increasing demand for the higher integration density, the problem as follows has been found out. That is, when polishing the copper film by the CMP method, the film between wiring layers, which is comprised of an SiOC film, and the stopper insulating film comprised of an SiO film, an SiN film or an SiCN film are separated from each other at the interface therebetween, and the manufacturing yield of the semiconductor device having the damascene wiring is lowered.

[0011]

An object of the present invention is to provide a technique capable of improving the reliability of the damascene wiring in which an SiOC film is used to form the insulating film in which the wiring trenches are formed or the insulating film in which the connection holes are formed.

[0012]

The above and other objects and novel characteristics of the present invention will be apparent from the description and the accompanying drawings of this specification.

[0013]

[Means for solving the Problems]

Outlines of the typical ones of the inventions disclosed in this application will be briefly described as follows.

[0014]

The present invention is a manufacturing method of damascene wirings, wherein the insulating film, in which the wiring trench is formed, and the insulating film, in which the connection hole is formed, are formed by the SiOC film and the SiC film with a thickness of 5 nm or more is laminated so as to come into contact with this SiOC film.

[0015]

[Embodiment of the Invention]

Hereinafter, embodiments of the present invention will be described in detail with reference to the accompanying drawings. Note that components having the same function are denoted by the same reference symbols throughout the drawings for describing the embodiments, and the repetitive description thereof is omitted.

[0016]

(First Embodiment)

The manufacturing method of the CMOSFET (Complementary Metal Oxide Semiconductor Field Effect Transistor) according to the first embodiment of the present invention will be described along the manufacturing process with reference to the sectional views in FIGs. 1 to 7 showing the principal part of the semiconductor substrate shown.

[0017]

First, as shown in FIG. 1, a semiconductor substrate 1 made of, for example, p^--single crystal silicon is prepared and device isolation regions 2 are formed on the main surface of the semiconductor substrate 1. Next, an impurity is ion-implanted with using a patterned photoresist film as a mask to form a p-well 3 and an n-well 4. A p-type impurity such as boron is ion-implanted into the p-well 3, and an n-type impurity such as phosphorus is ion-implanted into the n-well 4. Thereafter, the impurity for controlling the threshold of the MISFET (Metal Insulator Semiconductor FET) can be ion-implanted into the respective well regions.

[0018]

Next, a silicon oxide film to be a gate insulating film 5, a polycrystalline silicon film to be a gate electrode 6, and a silicon oxide film to be a cap insulating film 7 are sequentially deposited to form a laminated film, and then, the laminated film is etched with using a patterned photoresist film as a mask. In this manner, the gate insulating films 5, gate electrodes 6, and the cap insulating films 7 are formed.

[0019]

Next, after depositing a silicon oxide film by, for example, the CVD method, sidewall spaces 8 are formed on the sidewalls of the gate electrodes 6 by the anisotropic etching of this silicon oxide film. Thereafter, an n-type impurity such as phosphorus or arsenic is ion-implanted into the p-well 3 with using a photoresist film as a mask to form the n-type semiconductor regions 9 on both sides of the gate electrode 6 of the p-well 3. The n-type semiconductor regions 9 are formed in the self-alignment manner with respect to the gate electrode 6 and the sidewall spacers 8 and function as the source/drain of the n-channel MISFET. Similarly, a p-type impurity such as boron fluoride is ion-implanted into the n-well 4 with using a photoresist film as a mask to form the p-type semiconductor regions 10 on both sides of the gate electrode 6 of the n-well 4. The p-type semiconductor regions 10 are formed in the self-alignment manner with respect to the gate electrode 6 and the sidewall spacers 8 and function as the source/drain of the p-channel MISFET.

[0020]

Next, as shown in FIG. 2, after depositing a silicon oxide film on the semiconductor substrate 1 by the sputtering

method or the CVD method, the silicon oxide film is polished by the CMP method. By doing so, an interlayer insulating film 11 having a flat surface is formed. Subsequently, connection holes 12 are formed in the interlayer insulating film 11 by the etching with using a patterned photoresist film as a mask. The connection holes are formed at the required positions, for example, on the n-type semiconductor regions 9 or on the p-type semiconductor regions 10.

[0021]

Next, a titanium nitride film is formed on the entire surface of the semiconductor substrate 1 including the surface of the connection holes 12 by, for example, the CVD method, and then, a tungsten film to be filled into the connection holes 12 is formed by, for example, the CVD method. Thereafter, the tungsten film and the titanium nitride film in the region other than in the connection holes 12 are removed by, for example, the CMP method, thus forming the plugs 13 in the connection holes 12.

[0022]

Subsequently, a first wiring layer is formed by using the single damascene process. First, a stopper insulating film 14 is formed on the plugs 13 and a film between wiring layers 15 is formed. Since the first wiring layer described later is formed on the stopper insulating film 14 and the film between wiring layers 15, the total thickness thereof is determined depending on the design thickness necessary to the first wiring layer.

[0023]

The stopper insulating film 14 is a film serving as an

etching stopper in the process for forming the wiring trench in the film between wiring layers 15 and is made of a material having the etching selectivity with respect to the film between wiring layers 15. The stopper insulating film 14 is comprised of a silicon carbide (referred to as SiC, hereinafter) film with nitrogen content of 1% or less, and its thickness can be, for example, about 5 nm or larger. The SiC film is formed by, for example, the plasma CVD method under the conditions as follows. That is, the rf power is 200 to 1000 W, the pressure is 2 to 10 Torr, the temperature is 300 to 400°C, and the gas flow rate is 100 to 2000 sccm. The film between wiring layers 15 is comprised of an SiOC film and has a relative dielectric constant of about 3. Also, the SiOC is formed under the conditions as follows. That is, the rf power is 200 to 1000 W, the pressure is 2 to 10 Torr, the temperature is 300 to 400°C, and the gas flow rate is 100 to 2000 sccm.

[0024]

Note that the SiC film constituting the stopper insulating film 14 and the SiOC film constituting the film between wiring layers 15 can be formed with one plasma CVD apparatus. For example, the following two methods can be used: that is, the one in which the SiC film and the SiOC film are respectively formed in the two chambers provided in the plasma CVD apparatus; and the one in which the SiC film and the SiOC film are successively formed in the single chamber under different film forming conditions such as the gas to be used.

[0025]

Subsequently, wiring trenches 16 are formed in the predetermined regions of the stopper insulating film 14 and the

film between wiring layers 15 by the etching with using a patterned photoresist film as a mask.

[0026]

Next, a barrier metal layer 17 is formed over the entire surface of the semiconductor substrate 1 including the surfaces of the wiring trenches 16. The barrier metal layer 17 is comprised of, for example, a tantalum film and has a thickness of about 50 nm on the flat surface of the substrate. The tantalum film is formed by, for example, the sputtering method. It is also possible to form the barrier metal layer 17 with titanium nitride or tantalum nitride.

[0027]

Subsequently, a seed layer of copper (not shown) is formed on the barrier metal layer 17 by, for example, the CVD method or the sputtering method, and then, a copper film 18 is formed on the seed layer by the electroplating method.

[0028]

Next, as shown in FIG. 3, the copper film 18 and the seed layer are polished by the CMP method. Thereafter, the barrier metal layer 17 on the film between wiring layers 15 is removed by the further polishing. In this manner, the copper film 18 (including the seed layer) and the barrier metal layer 17 in the region other than the wiring trenches 16 are removed and the wiring 19 of the first wiring layer is formed.

[0029]

Incidentally, in the technique examined by the inventors of this invention in which the stopper insulating film is comprised of an SiO film, an SiN film or an SiCN film and the film between wiring layers is comprised of an SiOC film, the

stopper insulating film and the film between wiring layers are separated from each other at the interface thereof in the CMP process of the copper film and the barrier layer. However, in the first embodiment in which the stopper insulating film 14 is comprised of an SiC film and the film between wiring layers 15 is comprised of an SiOC film, the stopper insulating film (SiC film) 14 and the insulating film (SiOC film) 15 have been not separated from each other at the interface thereof in the CMP process of the copper film (including the seed layer) and the barrier metal layer 17.

[0030]

[Table 1]

Table 1

	SiOC	SiC	SiO	SiCN	SiN
Young's Modulus (GPa)	18	63	112	133	221
Stress (MPa)	47	62	-140	-245	-151
Nitrogen Content (%)	<1	<1	4	20	45

[0031]

The Young's modulus, stress, and nitrogen content of each insulating film are shown in Table 1. The adhesion between the SiOC film and each of the insulating films becomes smaller in the order of the SiN film, SiCN film, SiO film, and SiC film, and the adhesion to the SiOC film tends to depend on the nitrogen content. Also, the Young's modulus becomes smaller in the order of SiN film, SiCN film, SiO film, SiC film, and SiOC film. In addition, the SiOC film and the SiC film show the tensile stress, and on the other hand, the SiN film, the SiCN film, and the SiO film show the compressive stress.

[0032]

Judging from the above, it is thought that the molecular structure terminated by O and C enhances the bond between the molecules at the interface to improve the adhesion at the interface of the SiOC film. Furthermore, if the SiC film which has the tensile stress similar to the SiOC film, the difference in Young's modulus from the SiOC film of 50 GPa or less, and the difference in stress of 50 MPa or less is provided so as to come into contact with the SiOC film, the SiC film can relax the load in the horizontal and the vertical directions generated during the CMP process of the copper film, and thereby reducing the separation at the interface between the SiOC film and the SiC film.

[0033]

Note that the case where an SiC film is used as the stopper insulating film 14 has been exemplified here. However, it is also possible to form the stopper insulating film 14 with other insulating film if it has the difference in Young's modulus from the SiOC film of 50 GPa or less, or the difference in stress of 50 MPa or less. Also, the case where the SiC film constituting the stopper insulating film 14 is formed by the plasma CVD method and the film forming conditions have been exemplified here. However, the process and the film forming conditions are not limited to those described here.

[0034]

Next, a second wiring layer is formed by the dual damascene process. First, as shown in FIG. 4, a cap insulating film 20, an insulating film in which connection holes are to be formed (referred to as film between via layers, hereinafter) 21, and a stopper insulating film 22 for forming wiring are

sequentially formed on the wiring 19 of the first wiring layer.

[0035]

The cap insulating film 20 is comprised of an SiC film with a nitrogen content of 1% or less and a thickness of, for example, about 5 nm or larger. In addition, the cap insulating film 20 has a function to prevent the diffusion of copper. Also, it is made of a material having the etching selectivity with respect to the film between via layers 21 and is used as an etching stopper in the process for forming the connection holes in the film between via layers 21. The SiC film is formed by, for example, the plasma CVD method, and the film forming conditions approximately equal to those of the SiC film constituting the stopper insulating film 14 can be used.

[0036]

The film between via layers 21 is comprised of an SiOC film, the SiOC film is formed by, for example, the plasma CVD method, and the film forming conditions approximately equal to those of the SiOC film constituting the film between wiring layers 15 can be used.

[0037]

The stopper insulating film 22 is made of an insulating material having the etching selectivity with respect to a film between wiring layers deposited later on the film between via layers 21 and the stopper insulating film 22, and it is comprised of an SiC film with the nitrogen content of 1% or less with a thickness of, for example, about 5 nm or larger. The SiC film is formed by, for example, the plasma CVD method, and the film forming conditions approximately equal to those of the SiC film constituting the stopper insulating film 14 can be

used.

[0038]

Next, a photoresist film patterned into the hole shape is formed on the stopper insulating film 22, and the stopper insulating film 22 is etched with using the photoresist film as a mask.

[0039]

Subsequently, a film between wiring layers 23 is formed on the stopper insulating film 22. The film between wiring layers 23 is comprised of an SiOC film. The SiOC film is formed by, for example, the plasma CVD method, and the film forming conditions approximately equal to those of the SiOC film constituting the film between wiring layers 15 can be used. Note that, since wiring trenches to which the second wiring layer described later is filled are formed in the stopper insulating film 22 and the film between wiring layers 23, the total thickness thereof is determined depending on the design thickness necessary to the second wiring layer.

[0040]

Thereafter, as shown in FIG. 5, a photoresist film patterned into the trench shape is formed on a film between wiring layers 23, and the film between wiring layers 23 is etched with using the photoresist film as a mask. In this case, the cap insulating film 22 functions as an etching stopper film.

[0041]

Subsequently, the film between via layers 21 is etched with using the photoresist film and the stopper insulating film 22 as masks. In this case, the cap insulating film 20 functions as an etching stopper layer.

[0042]

Subsequently, the exposed cap insulating film 20 is removed by, for example, the dry etching method. Simultaneous with the removal of the cap insulating film 20, the stopper insulating film 22 is also removed. In this manner, the connection holes 24 are formed in the cap insulating film 20 and the film between via layers 21, and the wiring trenches 25 are formed in the stopper insulating film 22 and the film between wiring layers 23.

[0043]

Next, as shown in FIG. 6, a barrier metal layer 26 is formed over the entire surface of the semiconductor substrate 1 including the surfaces of the connection holes 24 and the wiring trenches 25. The barrier metal layer 26 is comprised of, for example, a tantalum film and has a thickness of, for example, about 50 nm over the flat surface of the substrate. The tantalum film is formed by, for example, the sputtering method. It is also possible to form the barrier metal layer 26 with titanium nitride and tantalum nitride.

[0044]

Subsequently, a seed layer (not shown) of copper is formed on the barrier metal layer 26 by, for example, the CVD method or the sputtering method, and a copper film 27 is formed on the seed layer by, for example, electroplating method.

[0045]

Next, as shown in FIG. 7, the copper film 27 and the seed layer are polished by the CMP method. Thereafter, the barrier metal layer 26 on the film between wiring layers 23 is removed by the further polishing. In this manner, the copper film 27

(including the seed layer) and the barrier metal layer 26 in the region other than the wiring trenches 25 are removed and the wiring 28 of the second wiring layer formed together with the connection member is formed.

[0046]

Also in the CMP process of this copper film 27 (including the seed layer) and the barrier metal layer 26, similar to the CMP process of the copper film 18 (including the seed layer) and the barrier metal layer 17, no separation has been caused at the interface between the cap insulating film (SiC film) 20 and the interlayer insulating film (SiOC film) 21, at the interface between the interlayer insulating (SiOC film) 21 and the stopper insulating film (SiC film) 22, and at the interface between the stopper insulating film (SiC film) 22 and the film between wiring layers (SiOC film) 23.

[0047]

Subsequently, though not shown, a cap insulating film 29 is formed on the wiring 28 of the second wiring layer, and after forming the wiring in the upper layer, the entire surface of the semiconductor substrate 1 is coated with a passivation layer. In this manner, the CMOSFET is approximately completed.

[0048]

Note that, although the CMOSFET is exemplified as the semiconductor device formed on the main surface of the semiconductor substrate 1 in the first embodiment, the semiconductor device formed on the main surface of the semiconductor substrate is not limited to this.

[0049]

Also, in the first embodiment, when forming the wiring 28

of the second wiring layer by the dual damascene process, the hole patterns are formed in the stopper insulating film 22 in advance and then the connection holes 24 in the film between via layers 21 and the wiring trenches 25 in the film between wiring layers 23 are simultaneously formed with using the cap insulating film 20 and the stopper insulating film 22 as etching stopper layers. However, the forming process is not limited to this. For example, the methods as follows are also available. That is: the method in which the connection holes 24 are formed in the film between wiring layers 23 and in the film between via layers 21 by the etching with using the photoresist film patterned into the hole shape as a mask and then the wiring trenches 24 are formed in the film between wiring layers 23 by the etching with using the photoresist film patterned into the trench shape as a mask; and the method in which the wiring trenches 25 are formed in the film between wiring layers 23 by the etching with using the photoresist film patterned into the trench shape as a mask and then the connection holes 24 are formed in the film between via layers 21 by the etching with using the photoresist film patterned into the hole shape as a mask.

[0050]

As described above, according to the first embodiment, in which the film between wiring layers 15, the film between wiring layers 23, and the film between via layers 21 are comprised of an SiOC film made of a material with a relatively low dielectric constant and the stopper insulating films 14 and 22 and the cap insulating film 20 in contact with the film between wiring layers 15, the film between wiring layers 23 and

the film between via layers 21 are comprised of an SiC film, it becomes possible to prevent the separation at the interface between the film between wiring layers 15 and the stopper insulating film 14 during the CMP process for forming the wiring 19 of the first wiring layer and the separation at the interface between the cap insulating film 20 and the film between via layers 21, at the interface between the film between via layers 21 and the stopper insulating film 22, and at the interface between the stopper insulating film 22 and the film between wiring layers 23 during the CMP process for forming the wiring 20 of the second wiring layer.

[0051]

(Second Embodiment)

The manufacturing method of the CMOSFET according to the second embodiment of the present invention will be described with reference to the sectional view in FIG. 8 showing the principal part of the semiconductor substrate.

[0052]

The case where the stopper insulating films 14 and 22 and the cap insulating film 20 are comprised of an SiC film has been described in the first embodiment. However, in this second embodiment, the stopper insulating films 14 and 22 and the cap insulating film 20 are comprised of an SiCN film A and an SiC film B, in which the SiCN film A can reduce the leakage current in comparison to the SiC film, and the SiC film B is interposed between the SiOC films constituting the film between wiring layers 15, the film between wiring layers 23, and the film between via layers 21 and the SiCN film A. The thickness of the SiCN film A is, for example, about 40 nm, and the thickness of

the SiC film B is, for example, about 10 nm. Also, the nitrogen content of the SiCN film A is 1% or larger.

[0053]

Also, the SiCN film A is formed by, for example, the plasma CVD method, and the film forming conditions thereof are as follows. That is, the rf power is 200 to 1000 W, the pressure is 2 to 10 Torr, the temperature is 300 to 400°C, and the gas flow rate is 100 to 2000 sccm. Also, the SiC film B is formed by, for example, the plasma CVD method, and the film forming conditions thereof are as follows. That is, the rf power is 200 to 1000 W, the pressure is 2 to 10 Torr, the temperature is 300 to 400°C, and the gas flow rate is 100 to 2000 sccm.

[0054]

As described above, in the second embodiment, the stopper insulating films 14 and 22 and the cap insulating film 20 are mainly comprised of the SiCN film A with relatively small leakage current and the SiC film B is interposed between the SiOC film, which constitutes the film between wiring layers 15, the film between wiring layers 23, and the film between via layers 21, and the SiCN film A. By doing so, it becomes possible to reduce the leakage current between the wirings and to prevent the separation of the SiOC film.

[0055]

(Third Embodiment)

In the third embodiment, an SiOC film which contains nitrogen is used to constitute the film between wiring layers 15, the film between wiring layers 23, and the film between via layers 21, and an SiCN film with relatively small leakage

current is used to constitute the stopper insulating films 14 and 22 and the cap insulating film 20. The SiOC film which contains nitrogen is formed by, for example, the plasma CVD method, and the film forming conditions thereof are as follows. That is, the rf power is 200 to 1000 W, the pressure is 2 to 10 Torr, the temperature is 300 to 400°C, and the gas flow rate is 100 to 2000 sccm. Also, the SiCN film is formed by, for example, the plasma CVD method, and the film forming conditions thereof are as follows. That is, the rf power is 200 to 1000 W, the pressure is 2 to 10 Torr, the temperature is 300 to 400°C, and the gas flow rate is 100 to 2000 sccm. The thickness of the SiCN film is, for example, about 50 nm.

[0056]

As described above, according to the third embodiment, the adhesion therebetween can be improved by containing nitrogen in the SiOC film. In this manner, it is possible to reduce the leakage current between the wirings and simultaneously to prevent the separation of the SiOC film.

[0057]

In the foregoing, the invention made by the inventors thereof has been concretely described based on the embodiments. However, it goes without saying that the present invention is not limited to the foregoing embodiments and the various changes and modifications can be made within the scope of the present invention.

[0058]

For example, in the above-mentioned embodiment, the case where the film made of low dielectric constant material is used to form the film between wiring layers and the film between via

layers of the damascene copper wiring has been described. However, the present invention is not limited to this. For example, even in the case where the interlayer insulating film made of a SiO film is formed on the wiring comprised of a refractory metal film such as aluminum alloy or tungsten formed by the use of, for example, the lithography technique and the dry etching process, the present invention can be applied to this interlayer insulating film.

[0059]

[Effect of the Invention]

The effect obtained by the typical ones of the inventions disclosed in this application will be briefly described as follows.

[0060]

In the damascene wiring in which an SiOC film is used to form an insulating film in which the wiring trenches are formed and an insulating film in which the connection holes are formed, an SiC film is used to form the stopper insulating film and the cap insulating film, alternatively, a laminated structure comprised of an SiCN film, an SiOC film, and an SiC film interposed between the SiCN film and the SiOC film is used to form the stopper insulating film and the cap insulating film. By doing so, it is possible to prevent the separation of the SiOC film. In this manner, it is possible to improve the reliability of the damascene wiring.

[Brief Description of the Drawings]

[FIG. 1]

A sectional view showing the principal part of a semiconductor substrate which illustrates the manufacturing

method of the CMOSFET according to the first embodiment of the present invention.

[FIG. 2]

A sectional view showing the principal part of the semiconductor substrate which illustrates the manufacturing method of the CMOSFET according to the first embodiment of the present invention.

[FIG. 3]

A sectional view showing the principal part of the semiconductor substrate which illustrates the manufacturing method of the CMOSFET according to the first embodiment of the present invention.

[FIG. 4]

A sectional view showing the principal part of the semiconductor substrate which illustrates the manufacturing method of the CMOSFET according to the first embodiment of the present invention.

[FIG. 5]

A sectional view showing the principal part of the semiconductor substrate which illustrates the manufacturing method of the CMOSFET according to the first embodiment of the present invention.

[FIG. 6]

A sectional view showing the principal part of the semiconductor substrate which illustrates the manufacturing method of the CMOSFET according to the first embodiment of the present invention.

[FIG. 7]

A sectional view showing the principal part of the

semiconductor substrate which illustrates the manufacturing method of the CMOSFET according to the first embodiment of the present invention.

[FIG. 8]

A sectional view showing the principal part of a semiconductor substrate which illustrates the manufacturing method of the CMOSFET according to the second embodiment of the present invention.

[Symbols]

1 semiconductor substrate
2 device isolation region
3 p-well
4 n-well
5 gate insulating film
6 gate electrode
7 cap insulating film
8 sidewall space
9 n-type semiconductor region
10 p-type semiconductor region
11 interlayer insulating film
12 connection hole
13 plug
14 stopper insulating film
15 film between wiring layers
16 wiring trench
17 barrier metal layer
18 copper film
19 wiring
20 cap insulating film

21 film between via layers

22 stopper insulating film

23 film between wiring layers

24 connection hole

25 wiring trench

26 barrier metal layer

27 copper film

28 wiring

A SiCN film

B SiC film

FIG. 1

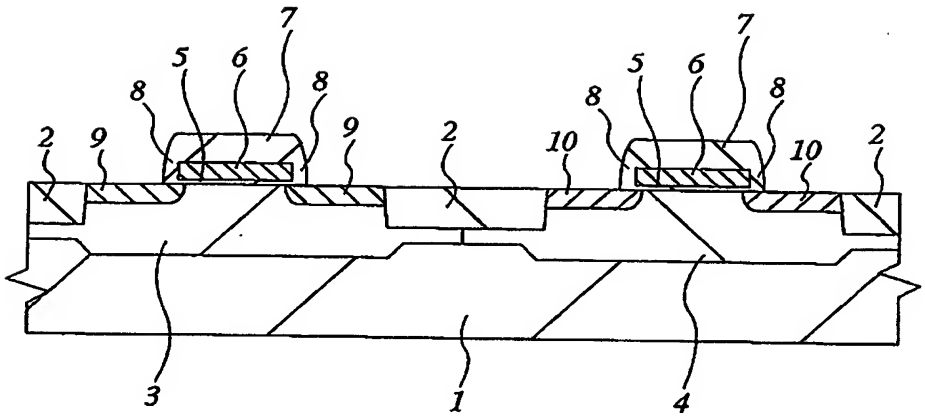
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FIG. 2

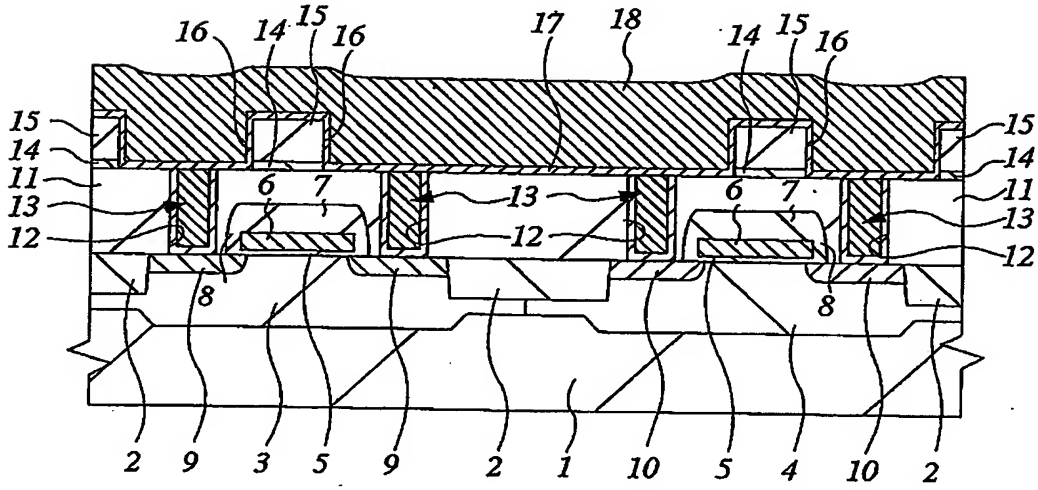
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FIG. 3

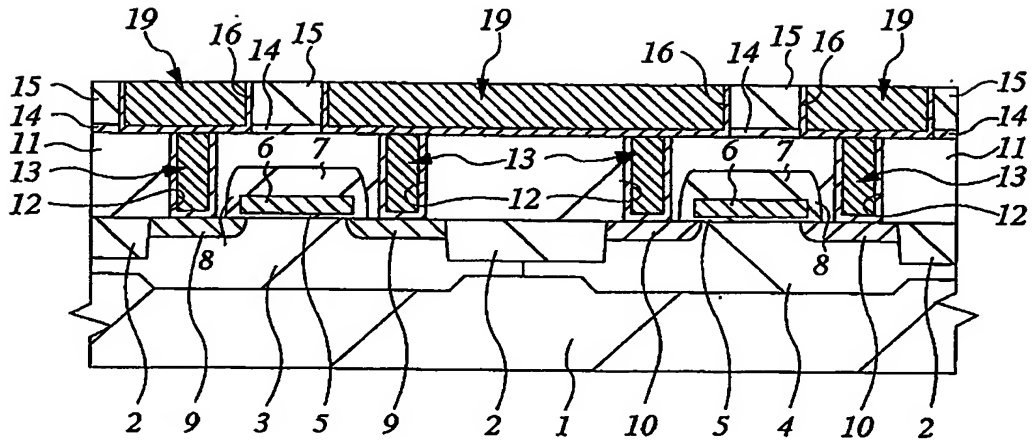
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FIG. 4

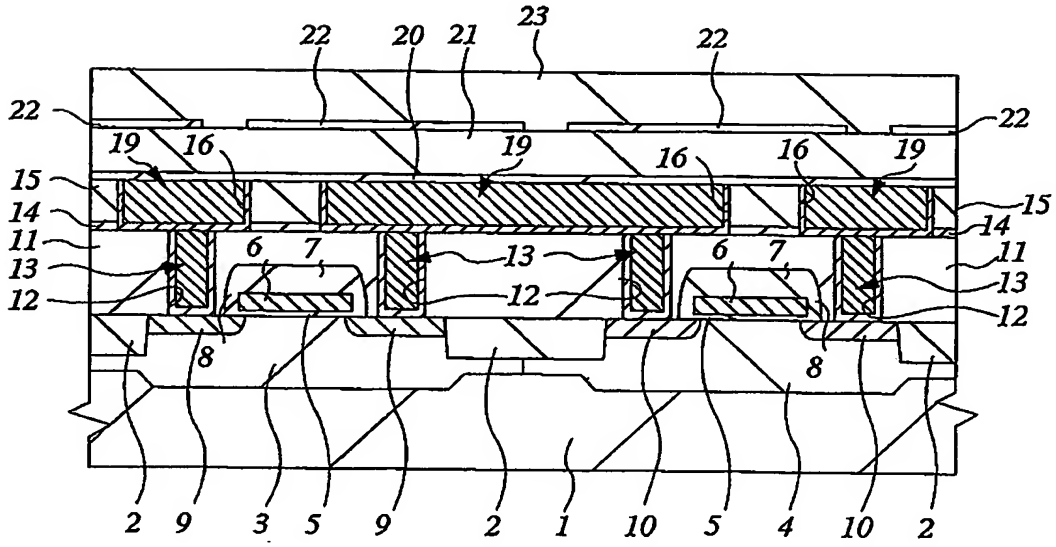
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FIG. 5

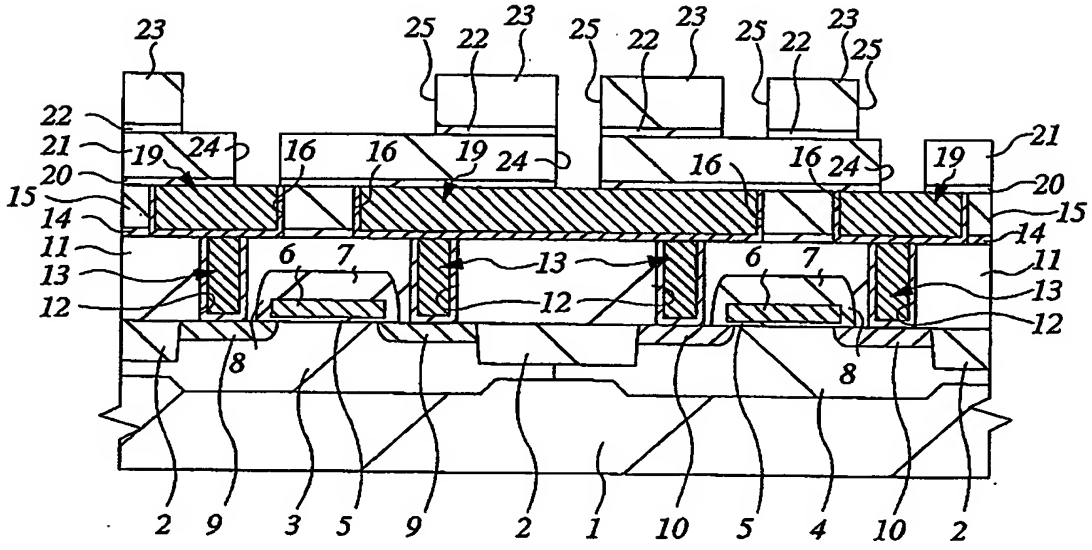
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FIG. 6

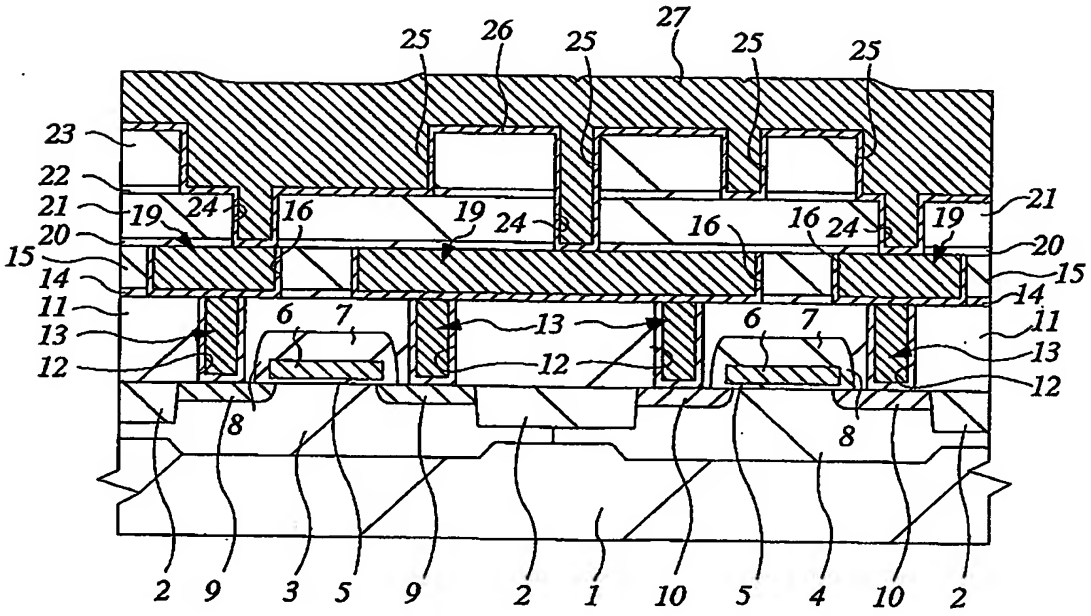
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FIG. 7

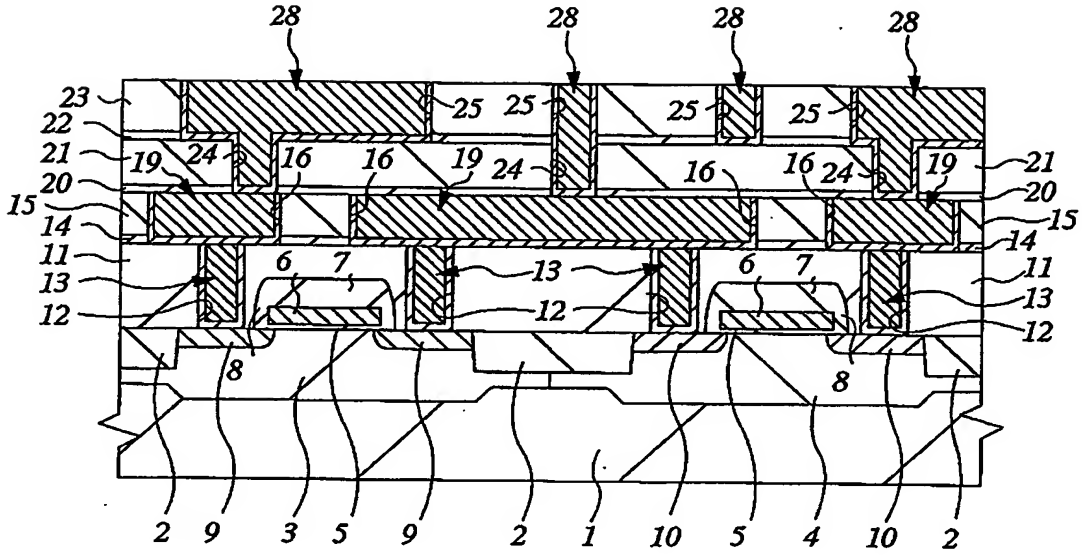
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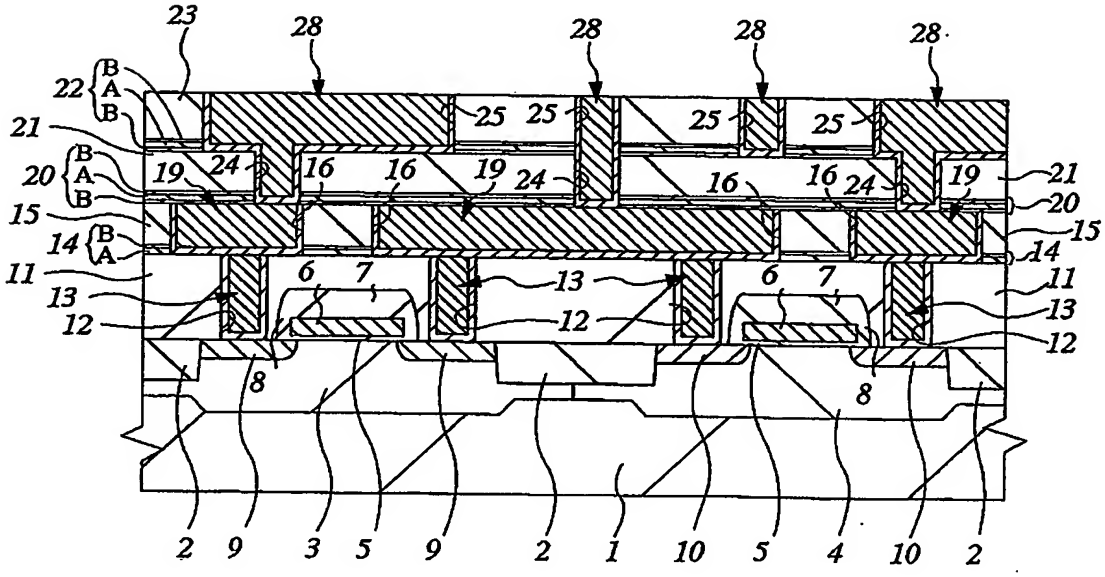
FIG. 8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[Document] Document of Abstract

[Abstract]

[Problems] Providing a technique capable of improving reliability of a damascene wiring that uses, as the SiOC films, the insulating film in which the wiring trench is formed and the insulating film in which the connection hole is formed.

[Means for solving the Problems] The stopper insulating films 14, 22 and the cap insulating film 20 are composed of: the SiCN film A capable of reducing the leakage current in comparison to the SiC film; and the SiC film B interposed between the SiOC film which constitutes the film between wiring layers 15, 23 and the film between via layers 21 and the above-mentioned SiCN film A.

[Selected Figure] FIG. 8